Curriculum Vitae/Resume

NARGES SHAHIDI

Computer Science and Engineering

Personal Information

Gender:	Female	Phone:	(+98)(21)44334285
Date of Birth:	1 Jun. 1985	www:	http://alum.sharif.edu/~nshahidi
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Education

Fall 2010 – Fall 2008 | M.Sc. in computer engineering, **Sharif University of Technology**
Major: Computer Architecture, GPA : 4/4 | Selected Courses
Thesis: "Segmented Reconfigurable Bus for SoCs"
Advisor: Prof. Hamid Sarbazi-Azad

Spring 2008 – Fall 2003 | B.Sc. in computer engineering, **Sharif University of Technology**
Major: Computer Software, GPA: 3.26/4 (3.57/4 for two last years)
Thesis: "Modeling and Evaluating of a Partial Adaptive Routing Algorithm for Mesh Interconnection Networks"
Advisor: Prof. Hamid Sarbazi-Azad

Honors

Jan. 2008	Rank 22 among nearly 13000 competitors in the national wide entrance exam for M.Sc. program in computer science.
Sep. 2003	Rank 106 among over 500,000 competitors in the national wide entrance exam for B.Sc. program in physics and mathematics.
Jun. 2002	Selected for the second step of student mathematic and computer olympiads.
Sep. 1996	Educated in the NODET (National Organization for Development Exceptional Talents) which is considered to be the best high school in Iran.

Publications

Nov. 2012 | **N. Shahidi**, A. Shafiee and A. Baniasadi, "*Heterogenous Interconnects for Low-Power Snoop-Based Chip Multiprocessors*", accepted to be appeared in JOLPE, Journal on Low Power Electronics.

Octobor 2010 | A. Shafiee, **N. Shahidi**, and A. Baniasadi, "*Helia: Heterogenous Interconnect for Low Resolution Cache Access*", in proceeding of 28th International Conference on Computer Design, Delft University, Amesterdam, The Netherlands, October 3-6, 2010.

May 2010 | A. Shafiee, **N. Shahidi**, and A. Baniasadi, "*Using Partial Tag Comparison in Low-Power Snoop Based Chip Multiprocessor*", in Workshop on Energy Efficient Design, held in conjunction with International Symposium on Computer Architecture (ISCA), St. Malo, France, May 20-25, 2010.

Research Interests

- Low Power Design
- Chip Multiprocessors
- Memory Systems
- Energy Efficient Storage Systems
- Reconfigurable System on Chip
- Network on Chip

Research Experiences

Jan 2011 Aug. 2008	Research Assistant working on Reconfigurable NoC, High Performance Computer Architecture & Networks (HPCAN) Lab, Sharif University of Technology, Supervisor: Prof. Hamid Sarbazi-Azad.
Jan 2011 Aug 2009	Research Assistant working on High-Performance Computing, School of Computer Science, Institute for Research in Fundamental Sciences (IPM), Supervisor: Prof. Hamid Sarbazi-Azad.
Aug 2009 Aug 2008	Research Assistant working on Chip-Multiprocessors, School of Computer Science, Institute for Research in Fundamental Sciences (IPM), Supervisor: Dr. Amirali Baniasadi.

Teaching Experiences

Instructor

Spring'11	Introduction to C/C++ Programming, **Imam-Khomeini International University**, Qazvin, Iran.

Teaching Assistant, Sharif University of Technology

Fall'10	Low Power Design, Instructor: Prof. Alireza Ejlali.
Summer'10	Computer Architecture Lab, Instructor: Prof. Hossein Asadi.
Fall'05	Introduction to Programming Languages, Instructor: Prof. Ali H. Abutalebi.

Work Experiences

Software/Firmware/Hardware Design Engineer in SiNA Microelectronic Co(SinaMicro).

Nov'12 – Mar'12

I have actively participated in design, development and functional verification of a pipelined RISC architecture for a 32-bit CPU called SABA. The core benefits from a 5-stage pipeline supporting a function-rich set of proprietarity as well as general instruction set. My responsibilities included the followings:

1. Flexible and scalable architectural design of the execution unit of SABA CPU.
2. Design and implementation of the datapath of the CPU at RTL level.
3. Development of a comprehensive low-level testbench for unit testing.
4. Deep investigation of timing cycles of instruction execution in the processor covering stalls and forwarding problems.
5. Assigning execution cycles for each instruction to proper stages of pipeline (scheduling) and test for functional integrity
6. Cooperation in functional checking of decoder unit for generation of proper control signals.
7. Cooperation in checking the controller unit for proper scheduling of the pipeline.
8. Cooperation in design and development of fetch and memory and writeback units of the processor.

Mar'12 – Mar'11

I used to work as a professional team member on a small-scale NGN project that targets an integrated gateway to provide multimedia communication ways among wireless and wired users locally and in a networked environment with different types of end devices.

1. Development of a management core for an Astrisk based soft-switch product.This management core is responsible for operation of the system and managing its various configurations and interfaces. Thorough knowledge of the software and hardware modules' functions was required for such a development. Also google's Protobuf format is used as communication and synchronization mechanism.
2. Development of software agents to facilitate management of the NGN system.
3. Set up different communication scenarios for the Asterisk based communication gateway.

I also used to work as a team member of a new release of SINA Radio Relay product that supports enhanced rates and configurations.

4. Developing an enhanced SNMP based Graphical User Interface for radio management.

Nov'08 – Nov'05

I used to work as a software design engineer in development of a Software-Defined Microwave Radio Relay. The system comprises of such essential parts as Linux operating system for control and management of system functions, a DSP-based base-band processing unit, and finally an RF unit as a front end for microwave communication. My job was to develop a graphical user interface to manage the whole system locally or remotely in the networked environment.

1. Developing SNMP-based Graphical User Interface for radio management. The software developed in JAVA using "swing" library and SNMP protocol is used to manage devices through the network. The user interface is employed to control the operation of the system in the network as well as managing/configuring specific links through the NMS mechanism.
2. Developing Quagga-based network management tool in radio management software.
3. Strengthening company's IT infrastructure. Setting up the SAMBA server, repositories and backup procedures in linux and windows environment.
4. Maintaining the company IT systems and software
5. Management of server software and associated backup routines

Presentations & Talks

Feb. 2011	Talk for a reading group at IPM (Institute for research in fundamental science): **Relaxed Memory Consistency Models**
Jan. 2011	M.Sc. Thesis Presentation: **Segmented Reconfigurable Bus for SoCs**.
Dec. 2009	In Storage Systems course: **Web Caches Management & Structures**
Jun. 2008	B.Sc. Thesis Presentation: **Performance Evaluation of Partially Adaptive Routing Algorithm for 2-D Mesh Networks**
Jun. 2006	In Software Engineering course: **Extreme Programming**

Major Accomplished Projects

Spring 2009	Synthesis and power analysis of Z77 and Huffman compression algorithm using Synopsis tool chain (Advanced VLSI course project).
Fall 2008	Design and implementation of combinatorial circuit test simulator (Testability course project).
Spring 2007	Developing software system for a library database (Software Engineering Lab project).
Spring 2007	Design and implementation of an indexer for Quick Test Retrieval of wikipedia pages including english and persian corpus (Modern information retrieval course project).
Fall 2006	Implementation of a compiler for MiniJava language (Compiler course project).
Spring 2006	Simulating the WiMAX network for Tehran with NS2 simulator (Network systems coarse project).
Fall 2005	Design and implementation of a disease classifier with a collection of machine learning algorithms (System analysis and design course project).
Fall 2004	Implementation of computer games: Arcade and Minesweeper (Advanced programming language course project).
Summer 2004	Design and simulation of single operand machine using C language (Assembly machine language course project).

Languages

English:	Fluent (TOEFL IBT: 90[R:28 L:21 S:23 W:18])
Farsi:	Mothertongue

Computer Skills

Simulators	Proficient in Interconnection Network Simulators: Booksim, WormSim, XMulator Proficient in SESC simulator for chip multiprocessors Mentor ModelSim© HDL simulator and vsim tcl scripting Simics© based full system computer architecture simulators (GEMS and Flexus) SimpleScalar simulator family Familiar with NS-2 and MATLAB
Design Tools	Synopsys Design Compiler©, Power Compiler© Familiar with Cadence SoC Encounter© physical design tool and Altra Quartus© FPGA design tools
Languages	Proficient in C/C++, Verilog, Java and C for CELL Processors Proficient in scripting languages like: Bash, AWK and PHP Familiar with VHDL, Assembly, C# and Python
DataBase	Proficient in MySql Familiar with SQL Server and Microsoft Access
OS	Proficient in different UNIX environments and MS Windows Familiar with Mac OS X
Other	LaTeXand MS Office

Selected Courses, Master of Science in Computer Architecture

Course	Grade from 20	Instructor
Testability	20	Prof. Hessabi
Advanced VLSI	18.5	Prof. Hessabi
Low Power Design	19.4	Prof. Ejlali
Interconnection Networks	17.7	Prof. Sarbazi-Azad
Storage System Design	18.7	Prof. Asadi

References

Hamid Sarbazi-Azad: Professor, Computer Engineering Department, Sharif University of Technology, Tehran, Iran. | Phone: +(98)(21) 6616-6622 | Email

Amirali Baniasadi: Associate Professor, Electrical and Computer Engineering Department, University of Victoia, Canada. | Phone: +(1)(250)721-8613 | Email

Shahin Hessabi: Associate Professor, Computer Engineering Department, Sharif University of Technology, Tehran, Iran. | Phone: +(98)(21)6616-4601 | Email

Farshad Baharvand: CEO, SiNA Microelectronics, Inc., Tehran, Iran. | Phone: +(98)(21)44954568 | Email